CLAIMS

We claim:

1. An interconnect structure comprising:

a substrate having first and second opposing surfaces and at least one internal side wall defining a through hole within said substrate extending from said first opposing surface to said second opposing surface;

a first conductive material positioned on said at least one internal side wall of said substrate;

a first conductive layer positioned on a portion of said first surface of said substrate, said first conductive layer having a first layer portion positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate;

a second conductive layer positioned on a portion of said second surface of said substrate, said second conductive layer having a first layer portion positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate;

a first dielectric layer positioned on said first conductive layer and said first opposing surface of said substrate and having at least one internal side wall defining an aperture in said first dielectric layer; and

a second conductive material positioned on said internal

side wall of said first dielectric layer and including a portion of said second conductive material positioned on and electrically connected to said first layer portion of said first conductive layer.

2. The interconnect structure of claim 1, wherein said first layer portion of said first conductive layer forms a seal over said first conductive material on said internal side wall of said substrate.

3. The interconnect structure of claim 1, wherein said first layer portion of said second conductive layer forms a seal over said first conductive material on said internal side wall of said substrate.

4. The interconnect structure of claim 1, wherein said seal comprises a metallurgical diffusion bond.

5. The interconnect structure of claim 1, further including a chip connector member having a portion thereof positioned on said second conductive material.

6. An interconnect structure comprising:

a substrate having first and second opposing surfaces and at least one internal side wall defining a through hole within said substrate extending from said first opposing surface to

said second opposing surface, wherein said substrate includes a metal layer between said first and second opposing surfaces and first and second non-conductive layers positioned, respectively, between said first opposing surface and said metal layer and between said second opposing surface and said metal layer;

a first conductive material positioned on said at least one internal side wall of said substrate;

a first conductive layer positioned on a portion of said first surface of said substrate, said first conductive layer having a first layer portion positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate;

a second conductive layer positioned on a portion of said second surface of said substrate, said second conductive layer having a first layer portion positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate;

a first dielectric layer positioned on said first conductive layer and said first opposing surface of said substrate and having at least one internal side wall defining an aperture in said first dielectric layer; and

a second conductive material positioned on said internal side wall of said first dielectric layer and including a portion of said second conductive material positioned on and electrically connected to said first layer portion of said first conductive layer.

7. The interconnect structure of claim 6, wherein said metal layer is selected from the group consisting of nickel, copper, molybdenum, iron, and alloys thereof.

8. The interconnect structure of claim 6, wherein said metal layer comprises copper-Invar-copper.

9. The interconnect structure of claim 6, further including a third conductive layer positioned substantially within said first non-conductive layer.

10. The interconnect structure of claim 9, further including a fourth conductive layer within said first non-conductive layer and positioned between said third conductive layer and said metal layer.

11. The interconnect structure of claim 10, wherein said fourth conductive layer comprises a first plurality of controlled impedance signal conductors.

12. The interconnect structure of claim 11, further including a fifth conductive layer positioned substantially within said second non-conductive layer.

13. The interconnect structure of claim 12, further including a sixth conductive layer positioned substantially within said second non-conductive layer and also positioned substantially between said fifth conductive layer and said metal layer.

14. The interconnect structure of claim 13, wherein said sixth conductive layer comprises a second plurality of controlled impedance signal conductors.

15. The interconnect structure of claim 6, wherein at least one of said first and second non-conductive layers includes an effective modulus to assure sufficient compliancy of said interconnect structure during operation.

16. The interconnect structure of claim 15, wherein said effective modulus is from about 0.01 Mpsi to about 0.50 Mpsi.

17. A method of forming an interconnect structure comprising the steps of:

providing a substrate having first and second opposing surfaces and at least one internal side wall defining a through hole within said substrate extending from said first opposing surface to said second opposing surface;

positioning a first conductive material on said at least one internal side wall of said substrate;

positioning a first conductive layer on a portion of said first surface of said substrate, said first conductive layer having a first layer portion positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate;

positioning a second conductive layer on a portion of said second surface of said substrate, said second conductive layer having a first layer portion positioned over said through hole and electrically connected to said first conductive material on said internal side wall of said substrate;

positioning a first dielectric layer on said first conductive layer and said first opposing surface of said substrate and having at least one internal side wall defining an aperture in said first dielectric layer; and

positioning a second conductive material on said internal side wall of said first dielectric layer and including a portion of said second conductive material positioned on and electrically connected to said first layer portion of said first conductive layer.

18. The method of making the interconnect structure of claim 17, wherein said step of providing said substrate having first and second opposing surfaces further comprises:

providing a metal layer between said first and second opposing surfaces of said substrate; and

positioning first and second non-conductive layers,

respectively, between said first opposing surface and said metal layer and between said second opposing surface and said metal layer.

19. The method of claim 17, wherein said step of positioning said first conductive layer on a portion of said first opposing surface of said substrate is accomplished by laminating said first conductive layer to said first opposing surface of said substrate, thereby sealing said first layer portion of said first conductive layer to said first conductive material on said internal side wall of said substrate.

20. The method of claim 17, wherein said step of positioning said second conductive layer on a portion of said second opposing surface of said substrate is accomplished by laminating said second conductive layer to said second opposing surface of said substrate, thereby sealing said first layer portion of said second conductive layer to said first conductive material on said internal side wall of said substrate.